REMARKS

Reconsideration and reexamination of this application in light of the above-amendments and the following remarks is respectfully requested. Claims 1-15, and 20-29 are pending in this application. By way of this response, claims 4, 6, 9, and 10 have been amended. Basis for the amendments can be found throughout the specification, claims, and drawings as originally filed. No new matter has been added. Reconsideration of the rejections set forth in the outstanding Office Action is respectfully requested in view of the preceding amended claims and the following remarks.

I. Allowable Subject Matter

Claims 4 and 10-15 stand objected to as being dependent upon a rejected based claim, but would be allowable if written in independent form including all of the limitations of the base claim and any intervening claims. Applicants greatly appreciate the indication of allowable subject matter, and have accordingly amended claims 4 and 10 to encompass the allowable subject matter. Thus, Applicants believe that claims 4 and 10-15

particularly point out and distinctly claim the present invention and respectfully request reconsideration and withdrawal of the objections set forth above.

II. Rejection Under 35 U.S.C. §112, Second Paragraph

Claim 4 stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter that Applicants regard as the invention. Applicants have amended claim 4 to provide antecedent basis for the phrase "second input terminal". In light of the above amendment, Applicants believe that claim 4 overcomes the rejection and respectfully requests withdrawal of the same.

III. Rejection Under 35 U.S.C. §102

Claims 1-3 and 5-9 stand rejected under 35 U.S.C. §102(e) as being anticipated by Abe. In light of the above amendments and the following remarks, Applicants respectfully traverse the rejection.

Claims 1-3, 5 and 7-8.

Applicant respectfully traverses the rejection of Claim 1. Applicant's invention of Claim 1 is directed to a method

for evaluating an input clock signal and generating an output clock signal based on the determination. Applicant's invention provides in combination with the other claimed elements determining whether the input clock signal is a differential clock signal or a single-ended clock signal.

The Abe reference discloses a system and method that evaluates one of two input clock signals, and based on that evaluation, generates an output clock signal based on the selected one of the two input clock signals. In contradistinction, Applicant's invention monitors a single input clock signal that is inputted on two terminals. The input clock signal is monitored to determine whether the input clock signal is a differential clock signal or a single-ended clock signal.

In addition, Abe's circuit evaluates one of the input signals to determine if an interruption, abnormality or clock changeover request has occurred. Applicant's claim 1 on the other hand, monitors the input clock signal to determine what type of signal is being input, a single-ended signal or a differential signal.

Thus as presently claimed, Applicant respectfully submits that Claims 1-3, 5, and 7-8 are not anticipated by Abe. Accordingly, Applicants respectfully request

reconsideration and withdrawal of this rejection of independent Claim 1 as well as dependent Claims 2-3, 5, and 7-8 under 35 U.S.C. §102(e).

Claim 6.

Claim 6 has been amended to clarify the scope of claim 6. Claim 6 defines a method that provides in combination with the other claimed elements receiving the first and second channel of an input clock signal and automatically generating a single-ended clock signal from either one of the channels or a combination of both channels.

As discussed above, Abe discloses a system and method that evaluates one of two input clock signals, and based on that evaluation, generates an output clock signal based on the selected one of the two input clock signals.

Thus as presently claimed, Applicant respectfully submits that Claim 6 is not anticipated by Abe. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection of independent Claim 6 under 35 U.S.C. §102(e).

Claim 9.

Claim 9 has been amended to clarify claim 9. Applicant's invention is directed to an apparatus that provides in combination with the other claimed elements first and second terminals for receiving first and second channels of an input clock signal. A detector outputs a clock mode signal as a function of the voltage potential of the clock signal second channel.

As discussed above, Abe discloses a system and method that evaluates one of two input clock signals, and based on that evaluation, generates an output clock signal based on the selected one of the two input clock signals.

Thus as presently claimed, Applicant respectfully submits that Claim 9 is not anticipated by Abe. Accordingly, Applicants respectfully requests reconsideration and withdrawal of this rejection of independent Claim 9 under 35 U.S.C. §102(e).

IV. Restriction Requirement

On October 18, 2001, Applicant filed a response to a restriction requirement selecting the invention of Group I which included Claims 1-15 and 20-29. In the present

office action, Claims 20-29 were indicated as being withdrawn from consideration and therefore were not examined. Applicant asserts that having selected Group I for examination, Claims 20-29 are pending in this application in addition to Claims 1-15, and requests that Claims 20-29 be examined.

V. Conclusion

Applicants have carefully reviewed each of the objections and rejections set forth, and have amended the claims as indicated herein to individually address the rejections and objections and to place all claims in condition for allowance. In view of the above, Applicants submit that the specification and drawings are in order and that all the claims are now in condition for allowance. Such action is respectfully requested. Enclosed is a check for $168 for the two independent claims. Please apply any other charges or credits to Deposit Account No. 06-1050. If the Examiner would like to discuss the matter further, the undersigned may be contacted at (858) 678-5070.

Attached is a marked-up version of the changes being made by the current amendment.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 4, 6, 9, and 10 have been amended as follows:

4. (Amended) [The method of claim 1,] A method comprising:

receiving an input clock signal representing either a differential clock signal or a single-ended clock signal;

determining whether the input clock signal is a differential clock signal or a single-ended clock signal; and

automatically generating an output clock signal based on the determination;

wherein receiving the input clock signal comprises receiving a single-ended clock signal on a first input terminal and a ground potential on [the] a second input terminal.

6. (Amended) A method comprising:

receiving a first channel of an input clock signal;

receiving a second channel of the input clock signal, wherein the second channel of the input clock signal is one of a constant signal at ground potential, a constant signal

above ground potential or a signal at the same frequency as the first channel of the input clock signal;

automatically generating a single-ended clock signal from the first and second channels of the input clock [signals] signal when the second channel of the input clock signal is one of a constant signal above ground potential or a signal at the same frequency as the first channel of the input clock signal; and

automatically generating a single-ended clock signal from the first channel of the input clock signal when the second channel of the input clock signal is a constant signal at ground potential.

9. (Amended) A device comprising:

a first terminal to receive a first channel of a clock input signal;

a second terminal to receive a second channel of the clock input signal; and

a detector coupled to the second terminal to receive the second channel of the clock input signal, wherein the detector is configured to output a clock mode signal as a function of a voltage potential of the second channel of the clock signal.

10. (Amended) [The device of claim 9 further comprising:] A device comprising:

a first terminal to receive a first clock input signal;

a second terminal to receive a second clock input signal;

a detector coupled to the second terminal to receive the second clock input signal, wherein the detector is configured to output a clock mode signal as a function of a voltage potential of the second clock signal;

a first circuit coupled to the first terminal configured to generate a first single-ended clock signal of the same frequency as the first clock input signal;

a second circuit coupled to the first terminal and to the second terminal to generate a second single-ended clock signal of the same frequency as the first clock input signal; and

a selector configured to select the first single-ended clock signal or the second single-ended clock signal based upon the clock mode signal.